PEC - Paraconsistent Electronic Circuits

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Abstract

In this work we present digital circuits (logical gates COMPLEMENT, AND, OR) inspired in a class of paraconsistent annotated logics $P\tau$. These circuits allow "inconsistent" signals in a nontrivial manner in their structure. Such circuits consist of six states; due the existence of literal operators to each of them, the underlying logic is functionally complete; it is a many-valued and paraconsistent (at least "semantically") logic.

Key words: Paraconsistency and implementing electronic circuits, paraconsistent logical gates, paraconsistent electronic circuits.

1 Introduction

In this work we present digital circuits (logical gates COMPLEMENT, AND, OR) inspired in a class of paraconsistent annotated logics $P\tau$ (see [Da Costa, Abe & Subrahmanian 91] and [Abe 92]). These circuits allow "inconsistent" signals in a nontrivial manner in their structure.

Such circuits consist of six states; due the existence of literal operators to each of them, the underlying logic is functionally complete (by a very known result due to [Rosser & Turquette 52]); it is a many-valued and paraconsistent (at least "semantically") logic.

The simulations were made at 50 MHz, 1.2 μm, by using the software *AIM-SPICE*, version 1.5a.

As far as we know, these results seem to be pioneering in using the concept of paraconsistency in the theory of electronic circuits. The applications appear to be large in horizon: it expands the scope of applications where conflicting signals are common,

such as in sensor circuits in robotics, industry automation circuits, race signal control in electronic circuits, and many other fields.

Let us consider a finite lattice of *truth-values* $\tau = <|\tau|, \leq>$, where $|\tau| = \{0, ½, ¼, ¾, 1, \top\}$. Intuitively, the elements of τ can be read:[1]

$½ \Rightarrow$ *undefined*

$1 \Rightarrow$ *true*

$0 \Rightarrow$ *false*

$¼ \Rightarrow$ *less false*

$¾ \Rightarrow$ *less true*

$\top \Rightarrow$ *inconsistent*

The underlying order is represented as follows

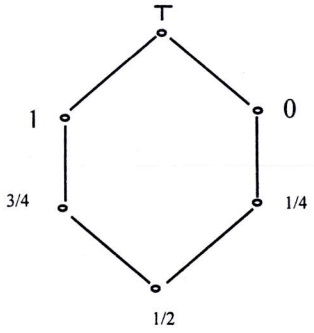


Figure 1 - Lattice *SIX*

We also define an operator $\sim: |\tau| \rightarrow |\tau|$ as $\sim(1) = 0$, $\sim(0) = 1$, $\sim(1/4) = 3/4$, $\sim(3/4) = 1/4$, $\sim(1/2) = 1/2$, $\sim(\top) = \top$. So, such operator has the "meaning" of negation.

The tension levels of the circuit and the logical values are described as follows:

Proposition	
Logical value	Tension
0	-4 volts
1	+4 volts

Annotation	
Logical value	Tension
0	- 4 volts
¼	- 2 volts
½	0 volts
¾	+ 2 volts
1	+ 4 volts
T	> +4 volts

Figure 2 – Logical values and tension levels

[1] We are aware that the terminology employed is unhappy, but we will keep them throughout in this paper.

2 Literal operators

Let us present the logical gates of the literal operators. Firstly, we introduce the literal operators *i, j. k, l, m,* ⊤.

Operator *i*

Input	Output
0	1
¼	0
½	0
¾	0
1	0
⊤	0

Operator *j*

Input	Output
0	0
¼	1
½	0
¾	0
1	0
⊤	0

Operator *k*

Input	Output
0	0
¼	0
½	1
¾	0
1	0
⊤	0

Operator *l*

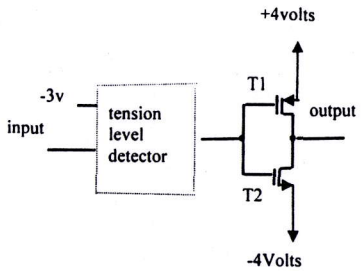
Input	Output
0	0
¼	0
½	0
¾	1
1	0
⊤	0

Operator *m*

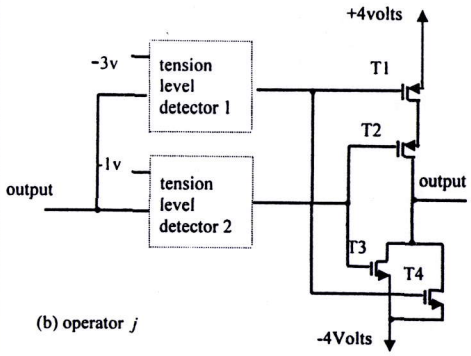
Input	Output
0	0
¼	0
½	0
¾	0
1	1
⊤	0

Operator *n*

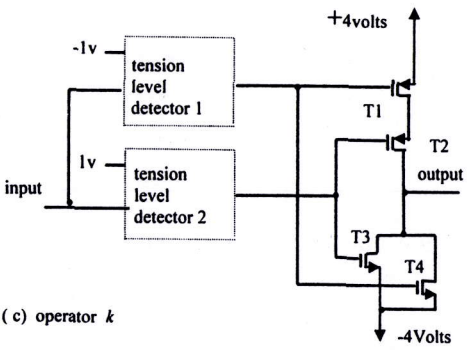
Input	Output
0	0
¼	0
½	0
¾	0
1	0
⊤	1



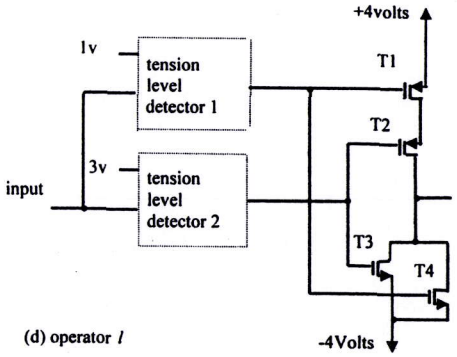
(a) operator *i*



(b) operator *j*



(c) operator *k*



(d) operator *l*

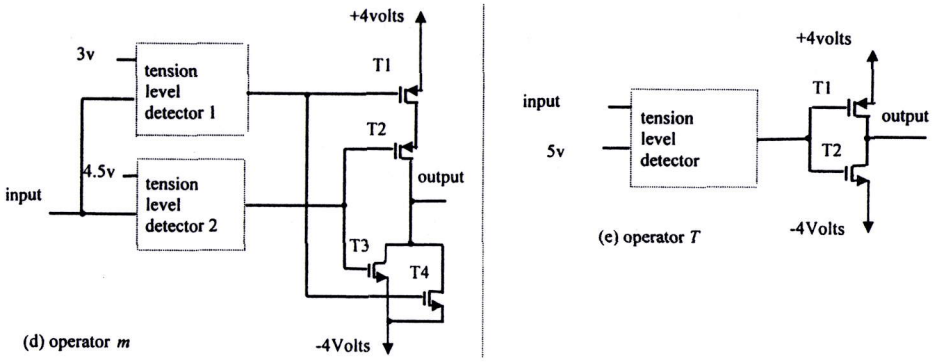


Figure 3 - Truth table and logical gates

3 Logical Gate Complement

Input	Output
0	1
¼	¾
½	½
¾	¼
1	0
T	T

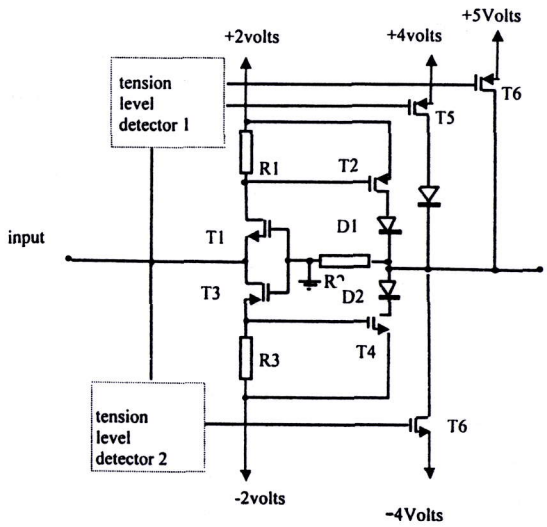


Figure 4 – Truth table and circuit of the operator Complement.

4 Logical gates AND and OR

AND

A	B	C
0	0	0
0	¼	0
0	½	0
0	¾	0
0	1	0
0	T	0
¼	0	0
¼	¼	¼
¼	½	¼
¼	¾	¼
¼	1	¼
¼	T	0
½	0	¼
½	¼	½
½	½	½
½	¾	½
½	1	½
½	T	0
¾	0	¼
¾	¼	¼
¾	½	½
¾	¾	¾
¾	1	¾
¾	T	¾
1	0	0
1	¼	¼
1	½	½
1	¾	¾
1	1	1
1	T	T
T	0	0
T	¼	¼
T	½	½
T	¾	¾
T	1	1
T	T	T

OR

A	B	C
0	0	0
0	¼	¼
0	½	½
0	¾	¾
0	1	1
0	T	T
¼	0	¼
¼	¼	¼
¼	½	½
¼	¾	¾
¼	1	1
¼	T	T
½	0	½
½	¼	½
½	½	½
½	¾	¾
½	1	1
½	T	T
¾	0	¾
¾	¼	¾
¾	½	¾
¾	¾	¾
¾	1	1
¾	T	T
1	0	1
1	¼	1
1	½	1
1	¾	1
1	1	1
1	T	T
T	0	T
T	¼	T
T	½	T
T	¾	T
T	1	T
T	T	T

Figure 5 – Truth table of the logical gates AND and OR

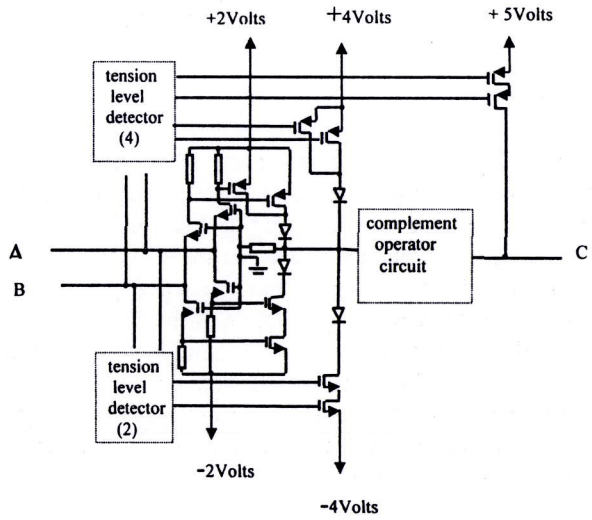


Figure 6 – Circuit of the logical gate AND

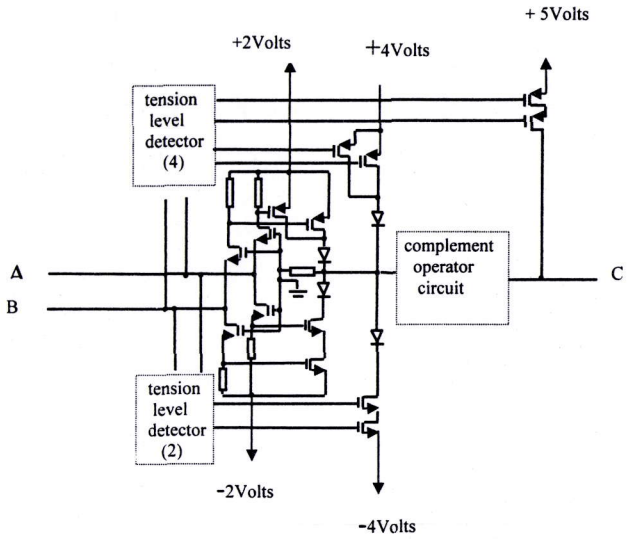


Figure 7 – Circuit of the logical gate OR

All the circuits were implemented by using the *CMOS* transistors. As we mentioned above, there exits an underlying logic such that these studies are functionally complete. So, any other circuits build can be expressed by the circuits AND and COMPLEMENT. Moreover, as an application we have considered a Paraconsistent Analyzer Module: it is a circuit that analyses signals detecting conflicting signals, and furnishes an adequate treatment to them. Details are in a forthcoming paper.

5 Simulations

The Figures 8, 9 and 10 bellow show us the simulation results made with the literal operator circuits, complement circuit, logical gates AND and OR, respectively. All circuits were implemented with *CMOS* transistors and simulated with AIMSPICE.

As it can be verified in the Figure 8, where it is presented the literal operators results, the 4 Volts output corresponds to the logical level 1. They are related exactly to the tension levels specified by the table of the Figure 2.

In the Figure 9, concerning complement operator, the output signal is the complemented signal applied in the input.

In the Figure 10, simulation of the logical circuits AND and OR, we can see that the results are the maximization and minimization according to the true table of the Figure 5.

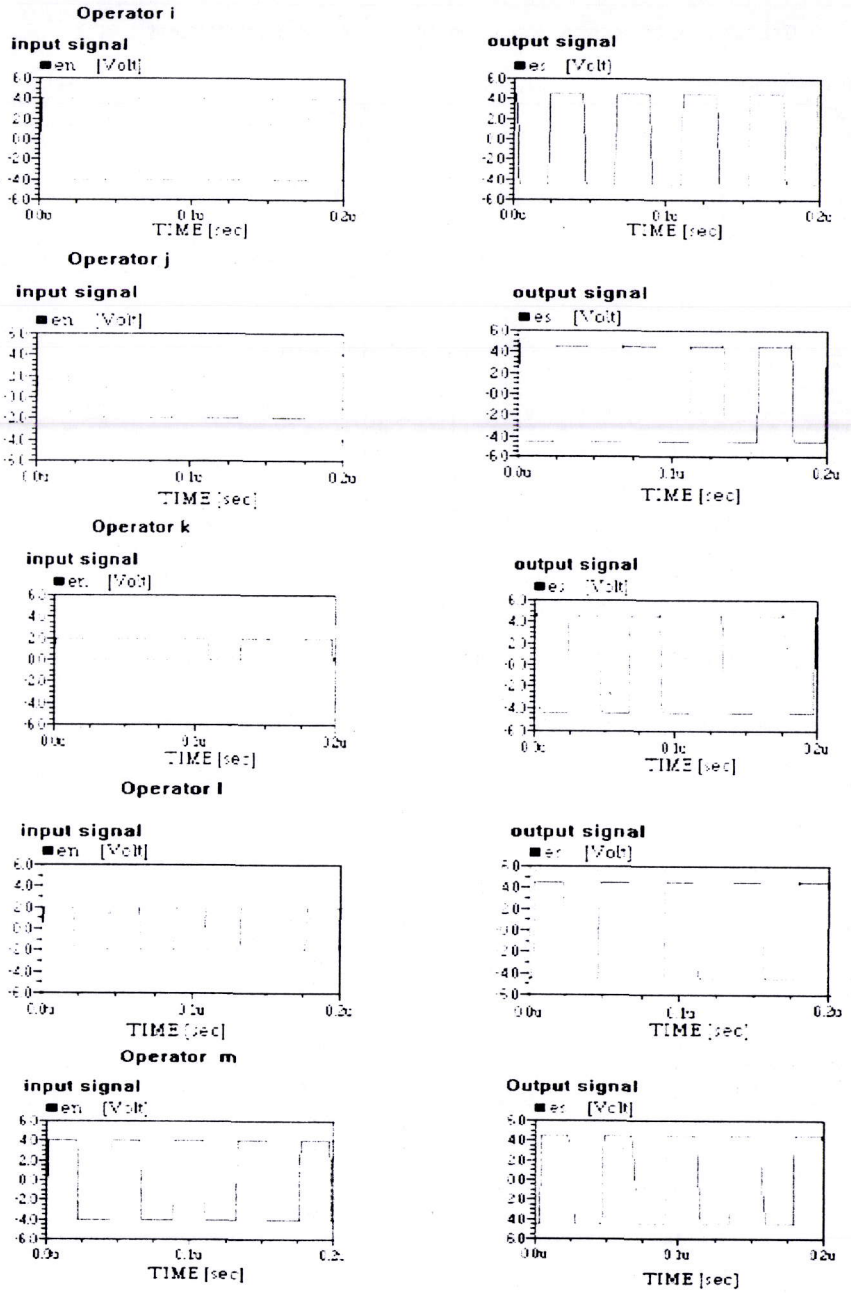


Figure 8 – Simulation results of the literal operators

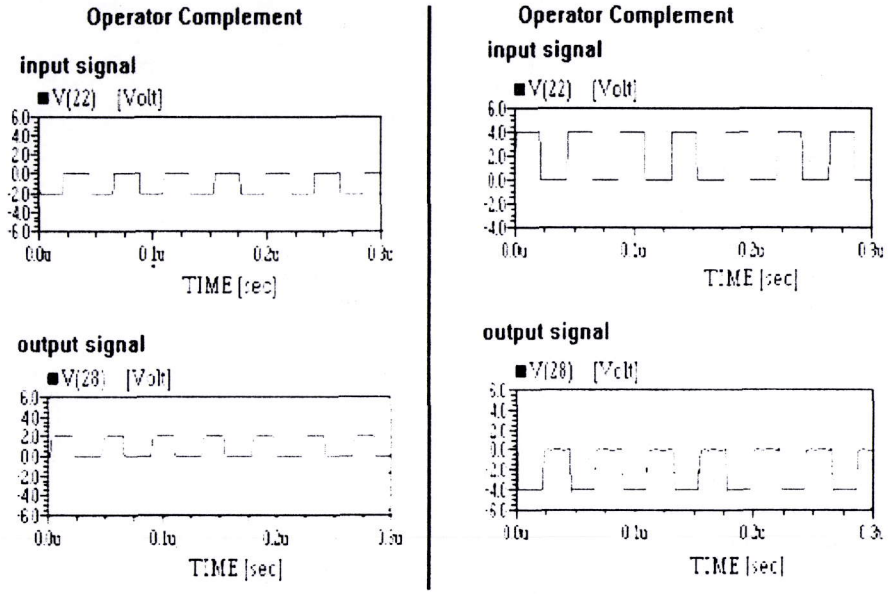


Figure 9 – Simulation results of the complement operator

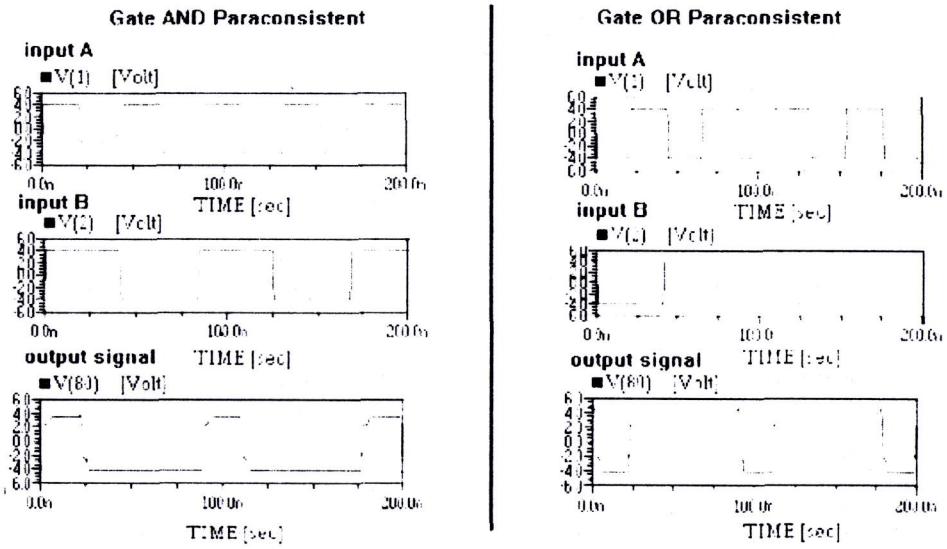


Figure 10 – Simulation results of the circuit logical gates AND and OR

6 Conclusions

We have implemented paraconsistent electronic circuits based on a class of paraconsistent annotated logics. As far as we know these studies are pioneering in the electronic circuit theory. The *PAM* shows the various applications that these circuits can have in several areas where conflicting situations are common: robotics, industry automation circuits, race signal control in electronic circuits, and many other fields, mainly in AI.

The paraconsistent logics give us the logical and philosophical bases to treat the concept of contradiction. This works came to establish that it is possible to materialize that concept physically trough suitable electronic circuits, opening a new branch of researching in this field.

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